Marko Bertogna – PhD, Associate Professor

Personal details

Born in Rijeka (Croatia) on October, 15th, 1977.

Nationality: Italian.

Email: marko.bertogna@unimore.it

Professional experience

From November 2014 **University of Modena** *Modena, Italy*
Associate Professor and leader of the High-Performance Real-Time (HiPeRT) Lab: http://hipert.unimore.it

November 2011 – October 2014 **University of Modena** *Modena, Italy*
Tenured Assistant Professor at the Algorithmic Research Group.

September 2009 – November 2011 **Scuola Superiore S.Anna** *Pisa, Italy*
Assistant Professor at the Real-Time Systems Laboratory of the Scuola Superiore Sant'Anna, Pisa.

April 2007 – September 2009 **Scuola Superiore S.Anna** *Pisa, Italy*
Two and a half years research contract.

January 2004 – May 2008 **Scuola Superiore S.Anna** *Pisa, Italy*
PhD student with a three-year scholarship. Research in the embedded real-time systems domain at the ReTiS lab (http://retis.sssup.it/).

September 2006 – January 2007 **UNC at Chapel Hill** *North Carolina, USA*
Visiting researcher at the University of North Carolina at Chapel Hill, collaborating with prof. Sanjoy Baruah (http://www.cs.unc.edu/~baruah/).

January 2003 – January 2004 **Scuola Superiore S.Anna** *Pisa, Italy*
One year research contract in the field of real-time systems. Analysis of Real-Time Operating Systems on FPGA platforms.

November 2001 – June 2002 **TU Delft / TU Eindhoven** *The Netherlands*
Research activity and design of integrated optical devices at the opto-electronic group of the Technische Universiteit of Delft and of Eindhoven. Scholarship of the University of Bologna.

Education

May 2008 **Scuola Superiore S.Anna** *Pisa, Italy*
Doctorate of Philosophy (score *100 cum laude)* with a dissertation entitled: "Real-Time Scheduling Analysis for Multiprocessor Platforms". The dissertation received the 2010 "Giovanni Spitali" Award for the best PhD thesis at the Scuola Superiore Sant'Anna of Pisa in 2008-2009.

July 2002 **University of Bologna** *Bologna, Italy*
Master in Telecommunication Engineering (score: *100 cum laude*).

1991-1996 **Liceo scientifico Belfiore** *Mantova, Italy*
Scientific high-school degree (score: *60/60*).

Research interests

Embedded real-time systems from theoretical models to practically relevant problems. Operating systems, hypervisors, and predictable execution models for next-generation multi-/many-core platforms. Co-scheduling algorithms for heterogeneous platforms with GPU or FPGA acceleration. Scheduling of next-generation high-performance real-time systems in ADAS/autonomous driving, avionic and industrial automation domains.

Honors and Awards

2010 Best Paper Award for the IEEE Transactions on Industrial Informatics (Impact Factor = 2,356) as the first author of the paper "*Resource-sharing servers for Open Environments*".

Outstanding Paper Award at the 24th International Conference on Real-Time Networks and Systems (RTNS'16), October 2016, Brest (France) for the paper *"Partitioning and Interface Synthesis in Hierarchical Multiprocessor Real-Time Systems"*.

Best Paper Award at the CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST'15), October 2015, Tehran (Iran) for the paper *"A Memory-Centric Approach to Enable Timing-Predictability within Embedded Many-Core Accelerators"*.

Outstanding Paper Award at the 27th Euromicro Conference on Real-Time Systems (ECRTS'15), June 2015, Lund (Sweden) for the paper *"Supporting Component-based Development in Partitioned Multiprocessor Real-Time Systems"*.

Best Paper Award at the 9th IEEE International Symposium on Industrial Embedded System (SIES 2014), June 2014, Pisa (Italy) for the paper *"Hard Constant Bandwidth Server: Comprehensive Formulation and Critical Scenarios"*.

Best Paper Award at the 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), August 2013, Taipei (Taiwan) for the paper *"Global Fixed Priority Scheduling with Deferred Pre-emption"*.

Best Paper Award at the 16th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2010), August 2010, Macau (China) for the paper *"Feasibility Analysis under Fixed Priority Scheduling with Fixed Preemption Points"*.

Best Paper Award at the 15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009), August 2009, Beijing (China) for the paper "*The Multi Supply Function Resource Abstraction for Multiprocessors: the Global EDF case*".

Best Paper Award at the 17th Euromicro Conference on Real-Time Systems (ECRTS'05), June 2005, Mallorca (Spain) as the first author of the paper *"Improved EDF multiprocessor schedulability analysis"*.

2010 "Giovanni Spitali" Award for the best PhD thesis of the Scuola Superiore Sant'Anna, Pisa, in 2008-2009.

Senior Member of the IEEE.

Board Member of the University of Mantova (Italy) since May 2017.

Communications Coordinator for Europe of the Technical Committee on Real-Time Systems (TCRTS) for 2011-2015.

Stakeholder Member of the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC).

Member of the Subcommittee on Real-Time Systems in Industrial and Factory Automation in IEEE-IES Technical Committee on Factory Automation (TCFA)

Member of the Editorial Board of the following journals:

- Co-editor of the Real-Time Systems Journal - Special Issue on Multicore Systems, 2015 (Springer).
- Since 2015: Open Access Computer Science Journal (PeerJ).
- Since 2013: International Journal of Embedded Systems (Inderscience Pusblishers).
- 2013-2016: The Scientific World Journal (Hindawi Publishing Corporation).

Chair of the following events:

- Smart Mobility Track Chair of 3rd International Forum on Research and Technologies for Society and Industry, (RTSI'17), Modena, Italy, September 11-13, 2017.
- Program Chair of the 28th Euromicro International Conference on Real-Time Systems (ECRTS'17), June 27-30, 2017, Dubrovnik, Croatia.
- Program Chair of the 21st International Conference on Reliable Software Technologies (Ada-Europe 2016), June13-17, 2016, Pisa, Italy.
- Program Chair of the 6th Real-Time Scheduling Open Problems Seminar (RTSOPS'15) held in conjunction with ECRTS'15: 27th Euromicro International Conference on Real-Time Systems, July 7-10, 2015, Lund, Sweden.
- Program Chair of the 20th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'15), Real-Time and (Networked) Embedded Systems Track, September 8-11, 2015, Luxembourg.
- Program Chair of the 5th Real-Time Scheduling Open Problems Seminar (RTSOPS'14) held in conjunction with ECRTS'14: 26th Euromicro International Conference on Real-Time Systems, July 8-11, 2014, Madrid, Spain.
- WiP Chair of the 26th Euromicro International Conference on Real-Time Systems, (ECRTS'14), July 8-11, 2014, Madrid, Spain.
- WiP Chair of the 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'13), April 9-11, 2013, Philadelphia, USA.
- Co-chair of the 1st Interdisciplinary Workshop on Algorithmic Challenges in Real-Time Systems (IWAC), 27-29 February 2012, Berlin, Germany.

Invited speaker at the following venues:

- Frontiers Conference. Title: "Are We Ready for Real Artificial Intelligence?" with Roberto Pieraccini (50 attendees). Vodafone Theater. Milan, Italy. September 21, 2017.
- TedX Modena: Failure as a Learning Experience. Title: "The Case of Autonomous Vehicles". Modena, Stocchi Theater (600 attendees). May 27, 2017.
- Italia Digitale. Title: "The Hercules Project and the Road towards Autonomous Driving". Milano, Gae Aulenti Auditorium (500 attendees). November 8, 2016.
- CRIT Research Seminar: the OPEN-NEXT Project. Title: "Multi-core Real-Time Systems" (80 attendees). Modena, Italy. June 30, 2016.
- Bosch Innovation. Title: "Predictable Multi-core Real-time Systems" (20 attendees). Renningen, Stuttgart, Germany. October 17, 2016.
- UPMARC 8th Summer School on Multicore Computing. Title: "Multi-core Real-Time Systems" (60 attendees). Uppsala, Sweden. June 6-9, 2016.
- ISEP/CISTER Distinguished Seminar Series. Title: "The Limited Preemption Scheduling Model" (50 attendees). Porto, Portugal, October 2nd, 2012.
- University of Luxembourg, Real-time Dependable Systems seminar series – FSTC/CSC-LASSY. Title: "EDF Scheduling for Identical Multiprocessor Systems" (50 attendees). Luxembourg. June 19th, 2012.
- INRIA/LORIA Nancy – TRIO research group. Title: "Limited Preemption Scheduling of Hard Real-Time Systems" (20 attendees). Amnéville, France. June 18th, 2012.

Member of the Program Committee of the following international conferences (in chronological order):

- 30th IEEE Real-Time Systems Symposium (RTSS'09), December 1-4, 2009, Washington DC, USA.
- 22nd Euromicro Conference on Real-Time Systems (ECRTS'10), July 7-9, 2010, Brussels, Belgium.
- 1st International Real-Time Scheduling Open Problems Seminar (RTSOPS'10), July 6, 2010, Brussels, Belgium.
- 16th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'10), WiP session, August 23, 2010, Macau, China.
- 31st IEEE Real-Time Systems Symposium (RTSS'10), WiP session, November 30 - December 3, 2010, San Diego, CA, USA.
- 17th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'11), WiP session, April 11-14, 2011, Chicago, IL, USA,
- 2nd International Real-Time Scheduling Open Problems Seminar (RTSOPS'11), July 5, 2011, Porto, Portugal.
- 32nd IEEE Real-Time Systems Symposium (RTSS'11), WiP session, November 29 - December 2, 2011, Vienna, Austria.
- 24th Euromicro Conference on Real-Time Systems (ECRTS'12), July 11-13, 2012, Pisa, Italy.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'12), in conjunction with 41th International Conference on Parallel Processing (ICPP'12), September 10 - 13, 2012, Pittsburgh, PA, USA.
- 17th IEEE International Conference on Emerging Technologies & Factory Automation (ETFA'12), Track 3: Real Time and Networked Embedded Systems, September 17-21, 2012, Krakow, Poland.
- 3rd International Real-Time Scheduling Open Problems Seminar (RTSOPS'12), July 10, 2012, Pisa, Italy.
- High-performance and Real-time Embedded Systems (HiRES) workshop, in conjunction with 8th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'13), January 21-23, 2013, Berlin, Germany.
- 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'13), Track 1: Applied Methodologies and Foundations, April 9-11, 2013, Philadelphia, USA.
- 25th Euromicro Conference on Real-Time Systems (ECRTS'13), July 9-12, 2013, Paris, France.
- 4th International Real-Time Scheduling Open Problems Seminar (RTSOPS'13), July 9, 2013, Paris, France.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'13) in conjunction with the 42nd International Conference on Parallel Processing (ICPP'13) October 1-4, 2013, Lyon, France.
- 21st International Conference on Real-Time and Network Systems (RTNS'13), 17-18 October 2013, Nice-Sophia Antipolis, France.
- 8th IEEE International Symposium on Industrial Embedded Systems (SIES '13), WiP session, June 19-21, 2013, Porto, Portugal.
- 18th IEEE International Conference on Emerging Technologies & Factory Automation (ETFA'13), Track on Real Time and Networked Embedded Systems, September 10-13, 2013, Cagliari, Italy.

- 34th IEEE Real-Time Systems Symposium (RTSS'13), WiP session, December 3-6, 2013, Vancouver, Canada.
- 2nd High-performance and Real-time Embedded Systems (HiRES'14) workshop, in conjunction with 9th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'14), January 20-22, 2014, Vienna, Austria.
- 20th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'14), WiP session, April 15-17, 2014, Berlin, Germany.
- 26th Euromicro Conference on Real-Time Systems (ECRTS'14), July 9-11, 2014, Madrid, Spain.
- 20th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'14), August 20-22, 2014, Chongqing, China.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'14) in conjunction with the 43rd International Conference on Parallel Processing (ICPP'14), September 9-12, 2014, Minneapolis, USA.
- 22nd International Conference on Real-Time and Network Systems (RTNS'14), October 8-10, 2014, Versailles, France.
- 2nd Workshop on Virtualization for Real-Time Embedded Systems (VtRES'14) in conjunction with the 19th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'14), September 16, 2014, Barcelona, Spain.
- 19th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'14), Track on Real Time and Networked Embedded Systems, September 16-19, 2014, Barcelona, Spain.
- 35th IEEE Real-Time Systems Symposium (RTSS'14), WiP session, December 2-5, 2014, Rome, Italy.
- 21st IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'15), April 2015, Seattle, Washington, USA.
- 27th Euromicro International Conference on Real-Time Systems (ECRTS'15), July 7-10, 2015, Lund, Sweden.
- 3rd High-performance and Real-time Embedded Systems (HiRES'15) workshop, in conjunction with 10th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'15), January 19-21, 2015, Amsterdam, Netherlands.
- 21st IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'15), August 19-23, 2015, Hong Kong.
- International Workshop on Embedded Multicore Systems (ICPP-EMS'15) in conjunction with the 44th International Conference on Parallel Processing (ICPP'15), September 1-4, 2015, Beijing, China.
- 13th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC'15), Parallel and Distributed Systems Track, October 21-23, 2015, Porto, Portugal.
- 23rd International Conference on Real-Time and Network Systems (RTNS'15), November 4-6, 2015, Lille, France.
- 36th IEEE Real-Time Systems Symposium (RTSS'15), December 1-4, 2015, San Antonio, Texas, US
- 4th High-performance and Real-time Embedded Systems (HiRES'16) workshop, in conjunction with 11th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'16), January 18-20, 2016, Prague, Czech Republic.
- 19th Design, Automation and Test in Europe (DATE'16), Embedded Systems Software track - Real-time, Networked, and Dependable Systems, March 14-18, 2016, Dresden, Germany.

- 22nd IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'16), April 11-14, 2016, Vienna, Austria.
- 28th Euromicro International Conference on Real-Time Systems (ECRTS'16), July 5-8, 2016, Toulouse, France.
- International Workshop on Hardware/Software Interface for Internet of Things and Big Data (InterIoT&BigData'2016), in conjunction with International Conference on Parallel Processing (ICPP'2016), August 16-19, 2016, Philadelphia, PA, USA.
- 22nd IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'16), August 17-19, 2016, Daegu, Korea.
- 37th IEEE Real-Time Systems Symposium (RTSS'16), November 29-December 2, 2016, Porto, Portugal.

Reviewing activity

Reviewer for the following international journals:
IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Industrial Informatics, IEEE Transactions on Software Engineering, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, ACM Transactions on Embedded Computing Systems, ACM Operating Systems Review, Springer Real-Time Systems Journal, Springer Lecture Notes in Computer Science, Springer Journal of Scheduling, Springer Journal of Computer Science and Technology, Springer Journal of Signal Processing Systems, Springer International Journal on Software Tools for Technology Transfer, Elsevier Journal of Systems Architecture, Elsevier Journal of Computer and System Sciences, Elsevier Journal of Systems and Software, Elsevier Microprocessors and Microsystems, Elsevier Information Processing Letters, Hindawi Journal of Applied Mathematics, Wiley Software: Practice and Experience.

Reviewer for the following international conferences:
IEEE International Real-Time Systems Symposium (RTSS), IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), Euromicro Conference on Real-Time Systems (ECRTS), ACM Symposium On Applied Computing (SAC), IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS), and other minor conferences.

Reviewer for the following funding agencies/initiatives:

- Natural Sciences and Engineering Research Council of Canada (NSERC) - Discovery Grant (Canada) - Electrical and Computer Engineering (EG 1510).
- Italian Ministry for University and Research (MIUR) - SIR (Scientific Independence of young Researchers).

International projects

Coordinator of the EU project HERCULES: High-Performance Real-time Architectures for Low-Power Embedded Systems (H2020/ICT/2015/688860). Overall project budget: 3.261.299€ (2.780.923€ funded by EU and Switzerland). Budget assigned to the Research Unit of the University of Modena: 606.549€ (entirely funded by the EU).

Vice Coordinator and **Unit Leader** of the EU project CLASS Edge and CLoud Computation: A Highly Distributed Software Architecture for Big Data AnalyticS (H2020-ICT-2017-1). Overall project budget: 3.900.803€ (entirely funded by the EU). Budget assigned to the Research Unit of the University of Modena: 492.166€ (entirely funded by the EU).

Vice Coordinator and **Unit Leader** of the EU project P-SOCRATES: Parallel Software Framework for Time-Critical Many-Core Systems (FP7/2013/ICT/611016). Overall project budget: 3.624.9424€ (2.762.000€ funded by the EU). Budget assigned to the Research Unit of the University of Modena: 492.200€ (378.400€ funded by the EU).

Unit Leader of the EU project I-MECH: Intelligent Motion Control Platform for Smart Mechatronic Systems (H2020-ECSEL-2016/737453). Overall project budget: 17.003.102€ (5.018.645€ funded by the EU, 4.900.000€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 488.750€ (171.062€ funded by the EU, 146.625€ by the Italian Government).

Unit Leader of the EU project ENABLE-S3: European Initiative to Enable Validation for Highly Automated Safe and Secure Systems (H2020-ECSEL-2015/692455). Overall project budget: 68.135.913€ (16.651.856€ funded by the EU, 16.651.856€ by national authorities). Budget assigned to the Research Unit of the University of Modena: 216.563€ (86.625€ funded by the EU, 54.140€ by the Italian Government).

Unit Leader of the POR-FESR 2014-2020 project OPEN-NEXT: Open-source Software Templates for Next-Generation Industrial Embedded Platforms. Overall project budget: 1.021.250€ (739.250€ funded by the EU through the Emilia Romagna region). Budget assigned to the Research Unit of the University of Modena: 305.000€ (219.500€ funded by the EU through the Emilia Romagna region).

Unit Leader of a Technology Transfer Project (TTP) within EU project TETRACOM (FP7-ICT-2013/609491). TTP: SemBoost: order-of-magnitude performance Boost for a leading Semantic engine. Budget assigned to the Research Unit of the University of Modena: 70.000€ (30.000€ funded by the EU).

Management Committee (MC) Member for Italy of the EU project TACLe: Timing Analysis on Code-Level (ICT COST Action IC1202). Overall budget: 120.000€ (entirely funded by the EU).

Unit Leader of the EU project PREDATOR: Design for Predictability and Efficiency (FP7/2008/ICT/216008). Budget assigned to the Research Unit of Scuola Sant'Anna: 398.200€ (299.400€ funded by the EU).

Participant to the POR-FSE 2014-2020 project Automotive Academy: a learning by doing project for innovation in vehicle engineering. Funding of one research fellowship (by the EU through the Emilia Romagna region) for studies in the ADAS/autonomous driving domain.

Participant to the EU project ACTORS: Adaptivity and Control of Resources in Embedded Systems (FP7/2008/ICT/216586).

Participant to the EU project IRMOS: Interactive Realtime Multimedia Applications on Service Oriented Infrastructures (FP7/2007/ICT/214777).

Participant to the EU project FRESCOR: Framework for Real-time Embedded Systems based on Contracts (FP6/2005/IST/5-034026).

Industrial projects

Expert System s.p.a.: Parallelization and Performance Improvement of a C-based Semantic Engine. Overall budget: 36.600€ (entirely funded by the company). 18/7/2014 – 31/12/2014

Doxee s.r.l.: Performance Analysis of a Java-based Document Management Engine. Overall budget: 18.300€ (entirely funded by the company). 1/12/2014 – 31/5/2015

Doxee s.r.l.: Performance Optimization and Memory Occupancy Minimization of a Java-based Application for the Massive Production of Data-variable Documents on Multi-core Servers. Overall budget: 12.200€ (entirely funded by the company). 1/4/2016 – 31/7/2016

Egicon s.r.l.: Profiling of Real-Time Systems Executing upon an Embedded Multi-core Platform. Overall budget: 36.600€ (entirely funded by the company). 2/8/2016 – 31/8/2017

Doxee s.r.l.: Design and Implementation of a New Distributed On-demand Production System and Setup of a Competence Center on Document Composition. Overall budget: 91.500€ (entirely funded by the company). 01/09/2016 – 28/02/2018.

Nvidia Corporation: GPU Real-Time Computing and Scheduling. Overall budget: 114.198$ (entirely funded by the company). 20/03/2017 – 19/09/207.

SACMI Imola S.C.: Heterogeneous Multi-core Platforms for Real-Time Applications. Overall budget: 48.800€ (entirely funded by the company). 01/02/2017 – 31/1/2018.

Egicon Srl: Profiling of Real-Time Systems Executing on Multi-core Platforms. Overall budget: 36.600€ (entirely funded by the company). 02/08/2016 – 31/08/2017.

Bosch GmbH: funding of a 3-years PhD scholarship on Real-Time Multi-core Systems for Automotive Applications.

Magneti Marelli: co-funding of a post-doc contract on Real-Time Systems for ADAS applications.

Maserati: Machine Learning Methods for Automatic Classification of Handling Parameters

Tetra Pak: Real-time analysis and assessment of multi-core platforms for industrial motion and control.

Teaching activity

Responsible of the "**Real-Time Embedded Systems**" course (72 hours, 9 credits) for the Master Degree in Computer Engineering of the University of Modena, Italy, for the academic year 2017-2018.

Responsible of the "**Computer Architectures**" course (72 hours, 9 credits) for the Degree in Computer Science of the University of Modena, Italy, for the academic year 2017-2018.

Responsible of the "**Parallel Programming**" course (48 hours, 6 credits) for the Master Degree in Computer Science of the University of Modena, Italy, for the academic years 2016-2017, 2017-2018.

Course on "**Embedded Systems for Automotive**" (20 hours) for Alfa/Maserati's PD Training Program, batches January 2017, July 2017.

Responsible of three different courses on "**Computer Science**" (24 hours, 3 credits) for various degrees in 2015-2016 (3 classes), 2016-2017.

Teaching Assistant of the "**Basic Computer Science**" course (20 hours, 2 credits) for different degrees of the University of Modena, Italy, for the academic years 2012-2013 and 2013-2014, 2014-2015.

Responsible of the "**Computer Architectures**" course (94 hours, 9 credits) for the Degree in Automation Engineering of the University of Siena, Italy, for the academic year 2010-2011.

Responsible of the "**Real-Time Operating Systems**" course (52 hours, 5 credits) for the Degree in Automation Engineering of the University of Siena, Italy, for the academic years 2008-2009, 2009-2010 and 2010-2011.

Responsible of the "**Multiprocessor Scheduling**" course (2x10 hours, 2x1 credits) for PhD and Master students on Computer Science of the Scuola Sant'Anna, Pisa, Italy, for the academic year 2009-2010.

Responsible of the "**Multicore Systems**" course at the ERICSSON Research Center of Rome, Italy (16 hours), July 2008.

Personal life

Married with Lidia Maria Diaz Monzon (since September 2008).

Proud father of two children: Luca (April 22, 2010) and Diego (April 20, 2013).

Languages

Italian, English and Spanish: excellent level.

Croatian, German and French: good level.

Modena, September 1st, 2017
Marko Bertogna

Major publications

Marko Bertogna is author of more than 80 papers in international journals and peer-reviewed conferences, mainly in the field of real-time and embedded systems. His main interests are in the analysis and design of scheduling algorithms for single, multi- and many-core systems, protocols for the access to shared resources, resource-reservation techniques. His works collected more than 2000 citations, with an h-index of 25 (source: Google Scholar). A list of the major publications follows.

Books

1) Sanjoy Baruah, Marko Bertogna, Giorgio Buttazzo, "*Multiprocessor Scheduling for Real-Time Systems*", Springer International Publishing, Embedded Systems Series, 2015.

International Journals

2) Alessandra Melani, Marko Bertogna, Robert I. Davis, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio C. Buttazzo. *"Exact Response Time Analysis for Fixed Priority Memory-Processor Co-scheduling"*, IEEE Transactions on Computers. 66 (4), 631-646. April 2017.
3) Alessandra Melani, Marko Bertogna, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio C. Buttazzo. *"Schedulability Analysis of Conditional Parallel Task Graphs in Multicore Systems"*, IEEE Transactions on Computers. 66 (2), 339-353. February 2017.
4) Alessandro Biondi, Giorgio Buttazzo, Marko Bertogna, *"Schedulability Analysis of Hierarchical Real-Time Systems under Shared Resources"*, IEEE Transactions on Computers. 65(5): 1593-1605. May 2016.
5) Robert I. Davis, Liliana Cucu-Grosjean, Marko Bertogna, Alan Burns, *"A Review of Priority Assignment in Real-Time Systems"*, Elsevier Journal of Systems Architecture. 65(C): 64-82, April 2016.
6) Robert I. Davis, Marko Bertogna, Vincenzo Bonifaci, "*On the Compatibility of Exact Schedulability Tests for Global Fixed Priority Pre-emptive Scheduling with Audsley's Optimal Priority Assignment Algorithm*", Real-Time Systems: The International Journal of Time-Critical Computing. 52 (1): 113-122. January 2016. Springer.
7) Luís Miguel Pinho, Vincent Nélis, Patrick Meumeu Yomsi, Eduardo Quiñones, Marko Bertogna, Paolo Burgio, Andrea Marongiu, Claudio Scordino, Paolo Gai, Michele Ramponi, Michal Mardiak, "*P-SOCRATES: A parallel software framework for time-critical many-core systems"*, Microprocessors and Microsystems. 39 (8): 1190-1203. November 2015. Elsevier.
8) Robert Davis, Alan Burns, Jose Marinho, Vincent Nelis, Stefan Petter, Marko Bertogna. "*Global and Partitioned Multiprocessor Fixed Priority Scheduling with Deferred Pre-emption*", ACM Transactions on Embedded Computing Systems. 14 (3): Article 47, May 2015. ACM.
9) Giorgio Buttazzo, Marko Bertogna, Gang Yao. *"Limited Preemptive Scheduling for Real-Time Systems: a Survey"*, IEEE Transactions on Industrial Informatics. 9(1): 3-15. February 2013. IEEE.
10) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Feasibility Analysis under Fixed Priority Scheduling with Limited Preemptions"*, Real-Time Systems: The International Journal of Time-Critical Computing. 47(3): 198-223. May 2011. Springer.
11) Marko Bertogna, Sanjoy Baruah. *"Tests for global EDF schedulability analysis"*, Journal of Systems Architecture. 57(5): 487-497. May 2011. Elsevier.
12) Marko Bertogna, Sanjoy Baruah. *"Limited preemption EDF scheduling of sporadic task systems"*, IEEE Transactions on on Industrial Informatics. 6(4): 579-591. November 2010. IEEE.
13) Marko Bertogna, Nathan Fisher, Sanjoy Baruah. *"Resource-sharing servers for Open Environments"*, IEEE Transactions on Industrial Informatics. 5(3): 202-220. August 2009.IEEE. **Best paper award IEEE Transactions on Industrial Informatics 2010**.
14) Marko Bertogna, Michele Cirinei, Giuseppe Lipari. *"Schedulability analysis of global scheduling algorithms on multiprocessor platforms"*, IEEE Transactions on Parallel and Distributed Systems. 20(4): 553-566. April 2009. IEEE.

15) Marko Bertogna, Nathan Fisher, Sanjoy Baruah. *"Resource holding times: Computation and Optimization"*, Real-Time Systems: The International Journal of Time-Critical Computing. 41(2): 87-117. February 2009. Springer.
16) Thedor P. Baker, Michele Cirinei, Marko Bertogna. *"EDZL scheduling analysis"*, Real-Time Systems: The International Journal of Time-Critical Computing. 40(3): 264-289. Springer. December 2008.
17) Marko Bertogna, Michele Cirinei, Giuseppe Lipari. *"New schedulability tests for real-time task sets scheduled by Deadline Monotonic on multiprocessors"*, Lecture Notes in Computer Science. 3974/2006: 306-321. 2006. Elsevier.

Peer-Reviewed International Conferences

18) Nicola Capodieci, Roberto Cavicchioli, Paolo Valente and Marko Bertogna, "*SiGAMMA: Server based integrated GPU Arbitration Mechanism for Memory Accesses*", Proceedings of the 25th International Conference on Real-Time Networks and Systems (RTNS'17), Grenoble, France, October 2017.
19) Nicola Capodieci, Roberto Cavicchioli and Marko Bertogna, "*Memory Interference Characterization between CPU cores and integrated GPUs in Mixed-CriticalityPlatforms*". Proceedings of 22nd IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2017), Limassol, Cyprus, September 2017.
20) Marko Bertogna, Paolo Burgio, Giacomo Cabri and Nicola Capodieci, "*Adaptive Coordination in Autonomous Driving: Motivations and Perspectives*", Proceedings of the IEEE 26th International Conference on Enabling Technologies: Infrastructure for Collaborative Enterprises (WETICE'17), Poznan, Poland, August 2017.
21) Maria A. Serrano, Alessandra Melani, Sebastian Kehr, Marko Bertogna and Eduardo Quiñones, "*An Analysis of Lazy and Eager Limited Preemption Approaches under DAG-Based Global Fixed Priority Scheduling*", Proceedings of the 20th IEEE International Symposium on Real-Time Distributed Computing (ISORC'17), Toronto, Canada, May 2017.
22) Alessandra Melani, Maria A. Serrano, Marko Bertogna, Isabella Cerutti, Eduardo Quinones, Giorgio Buttazzo. *"A static scheduling approach to enable safety-critical OpenMP applications"*, Proceedings of the 22nd Asia and South Pacific Design Automation Conference (ASP-DAC 2017), Chiba/Tokyo, Japan, January 2017.
23) Alessandro Biondi, Giorgio C. Buttazzo, Marko Bertogna. *"Partitioning and Interface Synthesis in Hierarchical Multiprocessor Real-Time Systems"*, Proceedings of the 24th International Conference on Real-Time Networks and Systems (RTNS'16), Brest, France, October 2016. **Outstanding Paper Award.**
24) Ignacio Sañudo, Roberto Cavicchioli, Nicola Capodieci, Paolo Valente, Marko Bertogna. *"A Survey on Shared Disk I/O Management in Virtualized Environments under Real-Time Constraints"*, Proceedings of the Embedded Operating System Workshop (EWiLi'16), in conjunction with the Embedded Systems Week (ESWeek 2016), Pittsburgh PA, USA, October 2016.
25) Paolo Burgio, Marko Bertogna, Ignacio Sanudo Olmedo, Paolo Gai, Andrea Marongiu, Michal Sojka. *"A Software Stack for Next-Generation Automotive Systems on Many-core Heterogeneous Platforms"*, Proceedings of the 9th Euromicro Conference on Digital System Design (DSD 2016), Limassol, Cyprus, August-September 2016.
26) Ignacio Sanudo, Paolo Burgio and Marko Bertogna. *"Schedulability and Timing Analysis of Mixed Preemptive-Cooperative Tasks on a PartitionedMulti-Core System"* , Proceedings of the 7th International Workshop on Analysis Tools and Methodologies for Embedded and Real-Time Systems (WATERS'16), in conjuction with the 28th Euromicro Conference on Real-Time Systems (ECRTS 2016), Toulouse, France, July 2016.
27) Maria Serrano, Alessandra Melani, Marko Bertogna, Eduardo Quiñones. "*Response-Time Analysis of DAG Tasks under Fixed Priority Scheduling with Limited Preemption*" , Proceedings of the Design Automation and Test in Europe (DATE'16), Dresden, Germany, March 2016.
28) Alessandra Melani, Marko Bertogna, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio Buttazzo. "*Memory-Processor Co-Scheduling in Fixed Priority Systems*" , Proceedings of the 23rd International Conference on Real-Time Networks and Systems (RTNS'15), Lille, France, November 2015.

29) Abhilash Thekkilakattil, Robert I. Davis, Radu Dobrin, Sasikumar Punnekkat, Marko Bertogna. "*Multiprocessor Fixed Priority Scheduling with LimitedPreemptions*" , Proceedings of the 23rd International Conference on Real-Time Networks and Systems (RTNS'15), Lille, France, November 2015.
30) Paolo Burgio, Andrea Marongiu, Paolo Valente and Marko Bertogna. "*A memory-centric approach to enable timing-predictability within embedded many-core accelerators*". The CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST'15), Tehran, Iran, October 2015. **Best Paper Award**.
31) Maria A. Serrano, Alessandra Melani, Roberto Vargas, Andrea Marongiu, Marko Bertogna and Eduardo Quinones. "*Timing Characterization of OpenMP4 Tasking Model*", Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES'15), Amsterdam, The Netherlands, October 2015.
32) Alessandra Melani, Marko Bertogna, Vincenzo Bonifaci, Alberto Marchetti-Spaccamela, Giorgio C. Buttazzo. "*Response-Time Analysis of Conditional DAG Tasks in Multiprocessor Systems*", Proceedings of 27th Euromicro Conference on Real-Time Systems (ECRTS 2015), Lund, Sweden, July 2015.
33) Alessandro Biondi, Giorgio C. Buttazzo, Marko Bertogna. "*Supporting Component-based Development in Partitioned Multiprocessor Real-Time Systems*", Proceedings of 27th Euromicro Conference on Real-Time Systems (ECRTS 2015), Lund, Sweden, July 2015. **Outstanding Paper Award.**
34) Vincent Nelis, Patrick Meumeu Yomsi, Luis Miguel Pinho, Eduardo Quiñones, Marko Bertogna, Andrea Marongiu, Paolo Gai and Claudio Scordino. "*A system model and stack for the parallelization of time-critical applications on many-core architectures*", Proceedings of 3rd High-performance and Real-time Embedded Systems (HiRES'15) workshop, in conjunction with 10th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'15), January 2015, Amsterdam, Netherlands.
35) Cláudio Maia, Marko Bertogna, Luís Nogueira, Luis Miguel Pinho, "*Response-Time Analysis of Synchronous Parallel Tasks in Multiprocessor Systems*", Proceedings of the 22nd International Conference on Real-Time Networks and Systems (RTNS'14), Versailles, France, October 2014.
36) Mario Bambagini, Marko Bertogna, Giorgio Buttazzo. "*On the Effectiveness of Energy-Aware Real-Time Scheduling Algorithms on Single-Core Platforms*", Proceedings of the 19th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2014), Barcelona, Spain, September 2014.
37) Luis Miguel Pinho, Eduardo Quinones, Marko Bertogna, Andrea Marongiu, Jorge Pereira Carlos, Claudio Scordino, Michele Ramponi, "*P-SOCRATES: a Parallel Software Framework for Time-Critical Many-Core Systems*", Proceedings of the 17th Euromicro Conference on Digital Systems Design (DSD 2014), Verona, Italy, August 2014.
38) Bo Peng, Nathan Fisher and Marko Bertogna, *"Explicit Preemption Placement for Real-Time Conditional Code"*, Proceedings of 26th Euromicro Conference on Real-Time Systems (ECRTS 2014), Madrid, Spain, July 2014.
39) Alessandro Biondi, Alessandra Melani, Marko Bertogna, Giorgio Buttazzo, *"Optimal Design for Reservation Servers under Shared Resources"*, Proceedings of 26th Euromicro Conference on Real-Time Systems (ECRTS 2014), Madrid, Spain, July 2014.
40) Vincent Nélis, Patrick Meumeu Yomsi, Luís Miguel Pinho, José Carlos Fonseca, Marko Bertogna, Eduardo Quiñones, Roberto Vargas, Andrea Marongiu, "The Challenge of Time-Predictability in Modern Many-core Architectures", Proceedings of 14th International Workshop on Worst-Case Execution Time Analysis (WCET 2014), Madrid, Spain, July 2014.
41) Alessandro Biondi, Alessandra Melani, Marko Bertogna, *"Hard Constant Bandwidth Server: Comprehensive Formulation and Critical Scenarios"*, Proceedings of 9th IEEE International Symposium on Industrial Embedded Systems (SIES 2014), Pisa, Italy, June 2014. **Best Paper Award**.
42) Luis Miguel Pinho, Eduardo Quinones, Marko Bertogna, Luca Benini, Jorge Pereira Carlos, Claudio Scordino, Michele Ramponi, *"Time Criticality Challenge in the Presence of Parallelised Execution"*, Proceedings of 2nd Workshop on High-performance and Real-time Embedded Systems (HiRES 2014), held in conjunction with the 9th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC 2014), Vienna, Austria, January 2014.

43) Jose Marinho, Vincent Nelis, Stefan M. Petters, Marko Bertogna, Robert I. Davis, *"Limited Pre-emptive Global Fixed Task Priority"*, Proceedings of 34th IEEE Real-Time Systems Symposium (RTSS 2013), Vancouver, Canada, December 2013.
44) Robert I. Davis, Alan Burns, Jose Marinho, Vincent Nelis, Stefan M. Petters, Marko Bertogna, *"Global Fixed Priority Scheduling with Deferred Pre-emption"*, Proceedings of the 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), Taipei (Taiwan), August 2013. **Best Paper Award**.
45) Cláudio Maia, Luís Nogueira, Luis Miguel Pinho, Marko Bertogna. *"Response-Time Analysis of Fork/Join Tasks in Multiprocessor Systems"*, WiP session of 25th Euromicro Conference on Real-Time Systems (ECRTS 2013), Paris, France, July 2013.
46) Mario Bambagini, Giorgio Buttazzo, Marko Bertogna. *"Energy-Aware Scheduling for Tasks with Mixed Energy Requirements"*, Proceedings of 4th International Real-Time Scheduling Open Problems Seminar (RTSOPS 2013), Paris, France, July 2013.
47) Rob Davis, Marko Bertogna. *"Optimal FP Scheduling with Deferred Preemptions"*, Proceedings of 11th Workshop on Models and Algorithms for Planning and Scheduling Problems (MAPSP 2013), Pont à Mousson, France, June 2013.
48) Mario Bambagini, Marko Bertogna, Mauro Marinoni, Giorgio Buttazzo. *"An Energy-Aware Algorithm Exploiting Limited Preemptive Scheduling under Fixed Priorities"*, Proceedings of 8th IEEE International Symposium on Industrial Embedded Systems (SIES 2013), Porto, Portugal, June 2013.
49) Mario Bambagini, Marko Bertogna, Mauro Marinoni, Giorgio Buttazzo. *"On the Impact of Runtime Overhead on Energy-Aware Scheduling"*, Workshop on Power, Energy, and Temperature Aware Real-time Systems (PETARS 2013), Philadelphia, USA, April 2013.
50) Giuseppe Lipari, Laurent George, Enrico Bini, Marko Bertogna. *"On the Average Complexity of the Processor Demand Analysis for Earliest Deadline Scheduling"*, Real-time systems: the past, present, and future, York, UK, March 2013.
51) Rob Davis, Marko Bertogna. *"Optimal Fixed Priority Scheduling with Deferred Pre-emption"*, Proceedings of 33rd IEEE Real-Time Systems Symposium (RTSS 2012), San Juan, Puerto Rico, December 2012.
52) Mario Bambagini, Giorgio Buttazzo, Marko Bertogna. *"Energy Saving Exploiting the Limited Preemption Task Model"*, Proceedings of 3rd International Real-Time Scheduling Open Problems Seminar (RTSOPS 12), Pisa, Italy, July 2012.
53) José Marinho, Stefan M. Petters and Marko Bertogna. *"Extending Fixed Task-Priority Schedulability by Interference Limitation"*, Proceedings of 20th International Conference on Real-Time and Network Systems (RTNS 2012), Pont à Mousson, France, November 2012.
54) Marko Bertogna, Giorgio Buttazzo, Gang Yao. *"Improving Feasibility of Fixed Priority Tasks using Non-Preemptive Regions"*, Proceedings of 32nd IEEE Real-Time Systems Symposium (RTSS 2011), Vienna, Austria, December 2011.
55) Marko Bertogna, Nathan Fisher. *"The Explicit Preemption Placement Problem for Real-Time Conditional Code"*, Proceedings of 2nd International Real-Time Scheduling Open Problems Seminar (RTSOPS 11), Porto, Portugal, July 2011.
56) Marko Bertogna, Orges Xhani, Mauro Marinoni, Francesco Esposito, Giorgio Buttazzo. *"Optimal Selection of Preemption Points to Minimize Preemption Overhead"*, Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS 11), Porto, Portugal, July 2011.
57) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Comparative evaluation of limited preemptive methods"*, Proceedings of the 15th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2010), Bilbao, Spain, September 2010.
58) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Feasibility Analysis under Fixed Priority Scheduling with Fixed Preemption Points"*, Proceedings of the 16th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2010), Macau, China, August 2010. **Best Paper Award**.
59) Marko Bertogna, Giorgio Buttazzo, Mauro Marinoni, Gang Yao, Francesco Esposito, Marco Caccamo. *"Preemption points placement for sporadic task sets"*, Proceedings of 22nd Euromicro Conference on Real-Time Systems (ECRTS 2010), Bruxelles, Belgium, June 2010.
60) Enrico Bini, Marko Bertogna, Sanjoy K. Baruah. *"The Parallel Supply Function Abstraction for a Virtual Multiprocessor"*, Proceedings of Dagsthul Seminar on Scheduling, Schloss Dagstuhl, Leibniz-Zentrum für Informatik, Germany, May 2010.

61) Tullio Facchinetti, Enrico Bini and Marko Bertogna. *"Reducing the Peak Power through Real-Time Scheduling Techniques in Cyber-Physical Energy Systems"*, International Workshop on Energy Aware Design and Analysis of Cyber Physical Systems (in conjunction with CPSWEEK 2010), Stockholm, Sweden, April 2010.
62) Dario Faggioli, Marko Bertogna, Fabio Checconi. *"Sporadic Server Revisited"*, Proceedings of 25th ACM Symposium On Applied Computing (SAC 2010), Sierre, Switzerland, March 2010.
63) Enrico Bini, Marko Bertogna, Sanjoy Baruah. *"Virtual Multiprocessor Platforms: Specification and Use"*, Proceedings of 30th IEEE Real-Time Systems Symposium (RTSS 2009), Washington, D.C., USA, December 2009.
64) Marko Bertogna. *"Evaluation of existing schedulability tests for global EDF"*, Proceedings of Real-time systems on multicore platforms: Theory and Practice (in conjunction with ICPP 2009), Vienna, Austria, September 2009.
65) Yifan Wu and Marko Bertogna. *"Improving Task Responsiveness with Limited Preemptions"*, Proceedings of 14th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2009), Palma de Mallorca, Spain, September 2009.
66) Gang Yao, Giorgio Buttazzo, Marko Bertogna. *"Bounding the Maximum Length of Non-Preemptive Regions Under Fixed Priority Scheduling"*, Proceedings of the 15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009), Beijing, China, August 2009.
67) Enrico Bini, Giorgio Buttazzo, Marko Bertogna. *"The Multi Supply Function Resource Abstraction for Multiprocessors: the Global EDF case"*, Proceedings of the 15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009), Beijing, China, August 2009. **Best Paper Award**.
68) Dario Faggioli, Michael Trimarchi, Fabio Checconi, Marko Bertogna, Antonio Mancina. *"An Implementation of the Earliest Deadline First Algorithm in Linux"*, Proceedings of the 24th Annual ACM Symposium on Applied Computing (SAC 2009), Honolulu, Hawaii, USA. March 2009.
69) Marko Bertogna, Fabio Checconi, Dario Faggioli. *"Non-Preemptive Access to Shared Resources in Hierarchical Real-Time Systems"*, Proceedings of the 1st Workshop on Compositional Theory and Technology for Real-Time Embedded Systems, Barcelona, Spain (Co-located with RTSS 2008). November 2008.
70) Marko Bertogna, Nathan Fisher and Sanjoy Baruah. *"Static-Priority Scheduling and Resource Hold Times"*, Proceedings of the 15th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2007), Long Beach, CA. March 2007.
71) Nathan Fisher, Marko Bertogna and Sanjoy Baruah. *"Resource-Locking Durations in EDF-Scheduled Systems"*, Proceedings of the 13th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2007), Bellevue, WA. April 2007.
72) Marko Bertogna and Michele Cirinei. *"Response-Time Analysis for Globally Scheduled Symmetric Multiprocessor Platforms"*, Proceedings of the 28th IEEE International Real-Time Systems Symposium (RTSS 2007), Tucson, Arizona. December 2007.
73) Nathan Fisher, Marko Bertogna and Sanjoy Baruah. *"The Design of an EDF-scheduled Resource-sharing Open Environment"*, Proceedings of the 28th IEEE International Real-Time Systems Symposium (RTSS 2007), Tucson, Arizona. December 2007.
74) Marko Bertogna, Michele Cirinei, Giuseppe Lipari, *"New schedulability tests for real-time task sets scheduled by Deadline Monotonic on multiprocessors"*, 9th International Conference on Principles of Distributed Systems (OPODIS 2005), Pisa (Italy), December 2005.
75) Marko Bertogna, Michele Cirinei, Giuseppe Lipari, *"Improved schedulability analysis of EDF on multiprocessor platforms"*, 17th Euromicro Conference on Real-Time Systems (ECRTS 2005), Mallorca (Spain), June 2005. **Best Paper Award**.
76) Babaud, Groen, Leijtens, M. Bertogna, J. den Besten, Barbarin, Oei, Karouta, Binsma, and M.K. Smit, *"First integrated continuously tunable AWG-based laser using electro-optical phase shifters"*, 12th European Conference on Integrated Optics (ECIO 2005), Grenoble, April 6-8, 2005.

Proceedings and Editorial

77) M. Bertogna. Proceedings of the *29th Euromicro Conference on Real-Time Systems (ECRTS 2017)*, Dubrovnik, Croatia, July 27-30, 2017.
78) M. Caccamo, M. Bertogna. *Special Issue on Multicore Systems.* Real-Time Systems, 52 (4). 2016.
79) M. Bertogna, L.M. Pinho, E. Quinones. Proceedings of the *21st Ada-Europe International Conference on Reliable Software Technologies* (Ada-Europe 2016), Pisa, Italy, June 13-17, 2016.
80) M. Bertogna, A. Easwaran. Proceedings of the *6th Real-Time Scheduling Open Problems Seminar* (RTSOPS'15), July 7-10, 2015, Lund, Sweden.
81) M. Bertogna. WiP Proceedings of the *26th Euromicro Conference on Real-Time Systems* (ECRTS 2014), Madrid, Spain, July 8-11, 2014.
82) M. Bertogna, S. Gopalakrishnan. Proceedings of the *5th Real-Time Scheduling Open Problems Seminar* (RTSOPS'14), July 8, 2014, Madrid, Spain.
83) M. Bertogna. WiP Proceedings of the *19th IEEE Real-Time and Embedded Technology and Applications Symposium*, Philadelphia, USA, April 9-11, 2013.

Approved EU Projects Deliverables

84) Marko Bertogna. "*Enhanced scheduler with migration support*", deliverable D3.3.2 for the EU-ICT project P-SOCRATES, March 2016.
85) Marko Bertogna. "*Overall Schedulability Analysis*", deliverable D4.3.2 for the EU-ICT project P-SOCRATES, March 2016.
86) Marko Bertogna. "*Independent Schedulability Analysis*", deliverable D4.3.1 for the EU-ICT project P-SOCRATES, March 2015.
87) Marko Bertogna. "*Simple Partitioned Scheduler*", deliverable D3.3.1 for the EU-ICT project P-SOCRATES, March 2015.
88) Marko Bertogna. "*Resource Allocation Requirements*", deliverable D3.1 for the EU-ICT project P-SOCRATES, April 2014.
89) Giorgio Buttazzo, Marko Bertogna, Gang Yao. *"Analysis of Preemptive and Non-Preemptive Scheduling"*, deliverable D3.4 for the EU-ICT project PREDATOR, January 2011.
90) Marko Bertogna. *"Handling Resource Constraints in Open Environments"*, deliverable D4c for the EU-ICT project ACTORS, January 2010.
91) Marko Bertogna. *"Resource reservation scheme evaluation"*, deliverable D4a for the EU-ICT project ACTORS, January 2009.

Book chapters

92) Sören Berger, Dominik Lamp, Manuel Stein, Thomas Voith, Tommaso Cucinotta, Marko Bertogna. *"Execution & Resource Management in QoS-aware Virtualized Infrastructures"*, in "Achieving Real-Time in Distributed Computing: From Grids to Clouds" ed. Dimosthenis Kyriazis, Theodora Varvarigou and Kleopatra G. Konstanteli, 200-217 (2012), IGI Global.

PhD Thesis

93) Marko Bertogna. *"Real-Time Scheduling Analysis for Multiprocessor Platforms"*, Scuola Superiore Sant'Anna, Pisa, May 2008. Awarded with the **2010 "Giovanni Spitali" Award** for the best PhD thesis of the Scuola Superiore Sant'Anna, Pisa, in the years 2008 and 2009.

Technical Reports

94) Nathan Fisher, Marko Bertogna, Sanjoy Baruah. *"The Design of an EDF-scheduled Resource-sharing Open Environment"*, UNC-CS Tech Report, May 2007.

Master Thesis

95) *"InP-Based Integration of Semiconductor Optical Amplifier and Phase Modulators"*, University of Bologna / Technische Universiteit Delft, July 2002.

Modena, September 1st, 2017
Marko Bertogna